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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:

Jung Chuan CHOU, et al. Appeal No.: Not yet assigned

Serial No.: **09/533,591** Group Art Unit: **2815**

Filed: **March 23, 2000** Examiner: **E. Ortiz**

Title: **A-WO_3-GATE ISFET DEVICES AND METHOD OF MAKING THE SAME**

TRANSMITTAL OF APPEAL BRIEF FOR THE APPELLANTS

Commissioner for Patents
Washington, D. C. 20231

January 13, 2003

Sir:

The amount of One Hundred and Sixty Dollars ($160.00) is enclosed to cover the official fees for this Appeal Brief. Please charge any fee deficiencies required with respect to this paper, or overpayment to our Deposit Account No. 50-2394.

Respectfully submitted,

IPS, Inc.

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Enclosure: Brief on Appeal

#14/Appeal Brief 1/23/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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In re the Application of: Appeal No.: Not yet assigned

Jung Chuan CHOU, et al. Confirmation No.: 1107

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BRIEF ON APPEAL

Commissioner for Patents
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Sir:

I. INTRODUCTION

This is an appeal from the Final Rejection of the Examiner dated June 19, 2002, finally rejecting Claims 1-11 in this application as being unpatentable over certain prior art under 35 U.S.C. §103. A Notice of Appeal was timely filed on November 19, 2002. Accordingly, this Brief is being timely filed.

II. REAL PARTY IN INTEREST

The real party in interest in the present application on appeal is National Yunlin University of Science and Technology of 123, Sec 3, University Road, Touliu, Yunlin, Taiwan, 640, R. O. C., by virtue of an Assignment recorded in the U.S. Patent and Trademark Office on June 7, 2000 at Reel 010864, Frame 0353.

III. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellant, appellant's representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

IV. STATUS OF CLAIMS

Claims 1-11 are pending, have been rejected and are being appealed.

V. STATUS OF AMENDMENTS

A Response after Final Rejection was filed on September 13, 2002. Response after Final Rejection did not result in allowance of the application. The Response after Final Rejection did not include amendments to the application.

VI. SUMMARY OF THE INVENTION

The claimed invention recites an amorphous WO_3 (a-WO_3) gated ion sensitive field effect transistor (ISFET). The ISFET includes a semiconductor substrate; a gate oxide layer on the semiconductor substrate; an amorphous WO_3 layer overlying the gate oxide layer to form a amorphous WO_3 gate; a source/drain in the semiconductor substrate beside the amorphous WO_3 gate; a metal wire on the source/drain; and a sealing layer overlying the metal wire, and exposing the amorphous WO_3 layer.

This present ISFET is very sensitive in solution, and particularly in acidic solution. The sensitivity of this present ISFET ranges from 50 to 58 mV/pH. Also, this ISFET has high linearity. Accordingly, this present ISFET is suitable to be applied to detect effluent.

VII. ISSUES ON APPEAL

The issue on appeal is whether Claims 1- 11 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over *Covington et al.*, U.S. Patent No. 4,502,938 (hereinafter *Covington*), in view of *Gardner et al.*, U.S. Patent No. 6,121,094 (hereinafter *Gardner*), all considered together.

VIII. GROUPING OF CLAIMS

Claim 1 is the independent claim, with claims 2-11 depending from claim 1. These claims all stand or fall together.

IX. APPELLANT'S ARGUMENTS

1) Amorphous-WO3 is not described in the cited prior art

Assuming for argument's sake, that *Gardner* compensates for deficiency of *Covington* regarding the use of WO_3 layer, the combined reference fails to teach amorphous WO_3. Moreover, Examiner admits that neither prior art reference discloses or suggests forming amorphous WO_3 as recited in claims 1 - 11.

2) Since Amorphous-WO3 is inconsistent with the cited prior art, it is therefore not obvious over it.

Examiner asserts that amorphous WO_3 is covered by *Gardner*, but Appellant strongly submits that this is an erroneous reading of the prior art, for the reason that the tungsten oxide

layer disclosed in *Gardner* cannot be of the amorphous form, since it cannot be produced by the heat treating process claimed by, and the illustrative embodiments disclosed in, *Gardner*.

Specifically, the Examiner states in the office action that "... the tungsten oxides layer taught by *Gardner* can be of an amorphous form or crystalline nature, depending on the use." However, this statement is simply erroneous, as discussed herein below.

Gardner's claims and all illustrative embodiments include a heat treating process to form a metal oxide layer. Hence, while *Gardner* states that materials used for the metal oxide layer are a matter of design choice, such materials are limited to those metal oxides which are formed by *Gardner*'s heat treating process.

Gardner teaches a semiconductor device comprising a gate dielectric layer, a conductor layer, and a metal oxide layer positioned between the gate dielectric layer and the conductor layer. *Gardner* further teaches that the metal oxide layer formed between the gate dielectric layer and the conductor layer can be tungsten oxide (WO_3). However, *Gardner* fails to point out or suggest anything about amorphous WO_3.

According to the disclosure in column 6, lines 26-34 of *Gardner*, the metal oxide layer 32, tungsten oxide, is formed by implanting oxygen into the tungsten conductor layer 35 to form the oxygen rich portion 34 and then carrying out a heat treating process to form the metal oxide layer 32 above the gate dielectric layer 18. However, one skilled in the art knows that after the heat treating process, e.g. a rapid thermal process or heating in a tube furnace as described in column 6, lines 31-34 of *Gardner*, the oxygen-rich tungsten layer 34 not only oxidizes as the tungsten

oxide layer 32, but also rearranges as a crystalline structure. It is well-known to those skilled in the art that the lattice of metal materials rearrange to crystallize after heat treatment or annealing.

Moreover, one of ordinary skill in the art, when referring to *Covington* in view of *Gardner* for forming a tungsten oxide layer on an ISFET device as a electroactive layer, can see that the resulting ISFET device will suffer from the current leakage of the polycrystallized or cystallized tungsten oxide layer.

It is noteworthy that:

A) *Gardner* does not mention amorphous WO_3, and

B) A heat treating process cannot produce amorphous WO_3. A heat treating process may form only crystalline or polycrystalline WO_3. Therefore, the use of amorphous WO_3 is not consistent with the *Gardner* invention.

3) Amorphous WO_3 is not combinable with *Gardner*'s method or illustrative embodiments

The Examiner states that to one versed in the art, the combined references suggest the claimed invention. However, there is simply no teaching or suggestion in either *Covington* or *Gardner* that would motivate one skilled in the art to combine such references.

Moreover, even if one skilled in the art would combine the references using impermissible hindsight, the teaching of the combined references would not be consistent with the claimed invention, particularly with respect to the heat-treating process included in *Gardner*'s claims and all illustrative embodiments.

4) Applicant's disclosure

The Examiner presents two citations from the Applicant's specification (page 5, lines 9-12), "The composition of the WO_3 layer and its properties vary with the selected method and condition during preparing the WO_3 layer. Most of the WO_3 layers are amorphous, polycrystalline or crystalline." and "It is well-known that WO_3 takes form of several structures, and within the various structures of the WO_3, different physical and chemical properties in terms of, e.g. resistivity and conductivity are present." The Examiner construes these statements to be an admission that the present invention, which makes use of a particular form of WO_3, is obvious. However, this is an erroneous conclusion.

While considerable variability exists with respect to the possible structures and properties of WO_3, it is the burden of the Examiner to show that the particular form and properties of the WO_3 in the context of the present invention are obvious in view of the prior art. And this has not been accomplished.

5) Summary and Conclusion

Amorphous WO_3 recited in independent claim 1 is not disclosed in any of the references cited by the Examiner. Moreover, it is not consistent with, and therefore unobvious over, the cited prior art references. For all of the reasons discussed above, it is respectfully submitted that the Examiner's final rejections of Claims 1- 11 are in error and should be reversed.

In the event that this paper is not being timely filed, the appellant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees which may be due with respect to this paper, may be charged to our Deposit Account No. 50-2394.

Respectfully submitted,

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Enclosure: Appendix A - Claims on Appeal

APPENDIX A

CLAIMS ON APPEAL

1. An a-WO_3 gate ISFET device, comprising:

a semiconductor substrate;

a gate oxide layer on the semiconductor substrate;

an a-WO_3 layer overlying the gate oxide layer to form an a-WO_3 gate;

a source/drain in the semiconductor substrate beside the a-WO_3 gate;

a metal wire on the source/drain; and

a sealing layer overlying the metal wire, and exposing the a-WO_3 layer.

2. The device as claimed in claim 1, wherein the length of the channel, the width of the channel and ratio of width/length of the channel of the ISFET is about 50μm, 100μm, and 20 respectively.

3. The device as claimed in claim 1, wherein the semiconductor substrate is P-type.

4. The device as claimed in claim 1, wherein the resistivity of the semiconductor substrate ranges from 8 to 12 Ω•cm.

5. The device as claimed in claim 1, wherein the lattice parameter of the semiconductor is (1,0,0).

6. The device as claimed in claim 1, wherein the thickness of the gate oxide is about 1000Å.

7. The device as claimed in claim 1, wherein the thickness of the tungsten oxide layer is at least 1000Å.

8. The device as claimed in claim 1, wherein the metal wire consists of Al.

9. The device as claimed in claim 1, wherein the sealing layer consists of epoxide resin.

10. The device as claimed in claim 1, wherein the source/drain is N-type.

11. The device as claimed in claim 10, wherein the N-type impurities within the source/drain consist of phosphorous.